

What is claimed is:

1. The architecture of a parallel computer comprising: a CPU module, a plurality of memory modules, each of which having a processor and RAM core, and a plurality of sets of buses that make connections between said CPU and memory modules and/or connections among memory modules, wherein the processors of the various memory modules operate on an instruction given by the CPU to the processors of the various memory, and wherein

said architecture of a parallel computer is constituted such that: a series of data having a stipulated relationship is given a space ID and the processor of each memory module manages a table that contains at least said space ID, the logical address of the portion of the series of data that it manages itself, the size of said portion and the size of the series of data, and,

the processor of each memory module determines if the portion of the series of data that it manages itself is involved in a received instruction, reads data stored in the RAM core and sends it out on a bus, writes data given via the bus to the RAM core, performs the necessary processing on the data, and/or updates said table.

2. The computer architecture according to claim 1, wherein

said processor has:

a space comparator that compares the space ID given by the CPU against the space ID of one or more series of data that it manages itself,

an address comparator that compares the logical address given by the CPU against the logical address of the portion of the data that it manages itself, and

an address calculator that calculates the physical address in its own RAM cell based on said logical address.

3. The computer architecture according to claim 1 or 2, wherein

each of said memory modules receives a synchronization signal for achieving synchronization with the CPU module and other memory modules, and

it is constituted such that it comprises input that is connectable to any of said plurality of sets of buses, and output that is connectable to any other of said plurality of sets of buses, and at least, it is able to output data according to said synchronization signal by connecting the input to one of said buses, inputting data and connecting the output to any of said other buses.

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4. The computer architecture according to claim 3, wherein

switches are provided on each of said sets of buses, thereby controlling the connections between said CPU module and the input or output of any of the memory modules, and/or between the input and output of one memory module and the output and input of another memory module, and

by switching said switches, the exchange of parallel data is achieved in each of said sets of buses.

5. The computer architecture according to claim 4, wherein the output of one memory module is connected to the input of another memory module via a first bus which is one of said plurality of sets of buses, and the output of said other memory module is connected to the input of still another memory module via a second bus which is another one of said plurality of sets of buses, so that the exchange of data over the first bus proceeds in parallel with the exchange of data over the second bus.

6. The computer architecture according to claim 5, wherein the connections between said bus and memory module are repeated to form multi-stage connections among memory modules.

7. The computer architecture according to any one of claims 1 through 6, wherein, when said processor receives an instruction to delete a specific element within a series of data, insert a specific element into said series of data, or add a specific element to the end of a series of data, said processor performs a table lookup, compares the region of data that it manages itself against the position of said element subject to deletion, insertion or addition, and based on the results of said comparison, updates the content of said table.

8. The computer architecture according to any one of claims 1 through 7, wherein, in response to a given instruction, said processor converts subscripts for specifying elements within a series of data, and/or executes value conversion for giving a specific modification to elements.

9. An information processing unit comprising: a CPU module, a plurality of memory modules, each of which having a processor and RAM core, and a plurality of sets of buses that make connections between said CPU and memory modules and/or connections among memory modules, wherein the processors of the various memory modules operate on an instruction given by the CPU to the processors of the various memory, and wherein

said information processing unit is constituted such that: a series of data having a stipulated relationship is given a space ID and the processor of each memory module

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manages a table that contains at least said space ID, the logical address of the portion of the series of data that it manages itself, the size of said portion and the size of the series of data, and,

5 the processor of each memory module determines if the portion of the series of data that it manages itself is involved in a received instruction, reads data stored in the RAM core and sends it out on a bus, writes data given via the bus to the RAM core, performs the necessary processing on the data, and/or updates said table.

10 10. The information processing unit according to claim 9, wherein said CPU module is constituted such that it can be linked to another bus that connects legacy memory, input devices and display devices to each other.

11. A computer system comprising the information processing unit according to claim 9 and one or more storage devices including legacy memory, input devices and display devices linked to the CPU module via another bus.